74HC4024

7-stage binary ripple counter

Rev. 03 — 12 November 2004 **Product data sheet**

1. General description

The 74HC4024 is a high-speed Si-gate CMOS device and is pin compatible with the 4024 of the 4000B series. The 74HC4024 is specified in compliance with JEDEC standard no. 7A.

The 74HC4024 is a 7-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q0 to Q6).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Applications

- Frequency dividing circuits
- Time delay circuits.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	C_L = 15 pF; V_{CC} = 5 V	-	14	-	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	90	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [1]	-	25	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4024N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC4024D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC4024DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC4024PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

6. Functional diagram

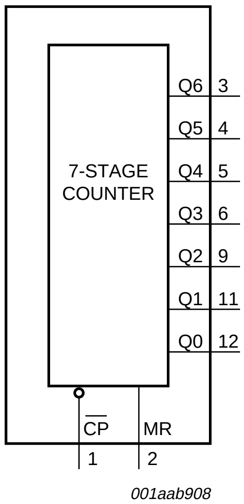


Fig 1. Functional diagram

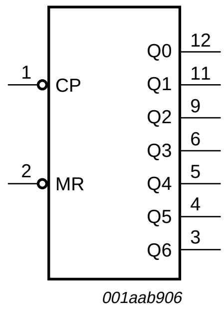


Fig 2. Logic symbol

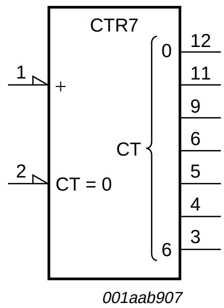


Fig 3. IEC logic symbol

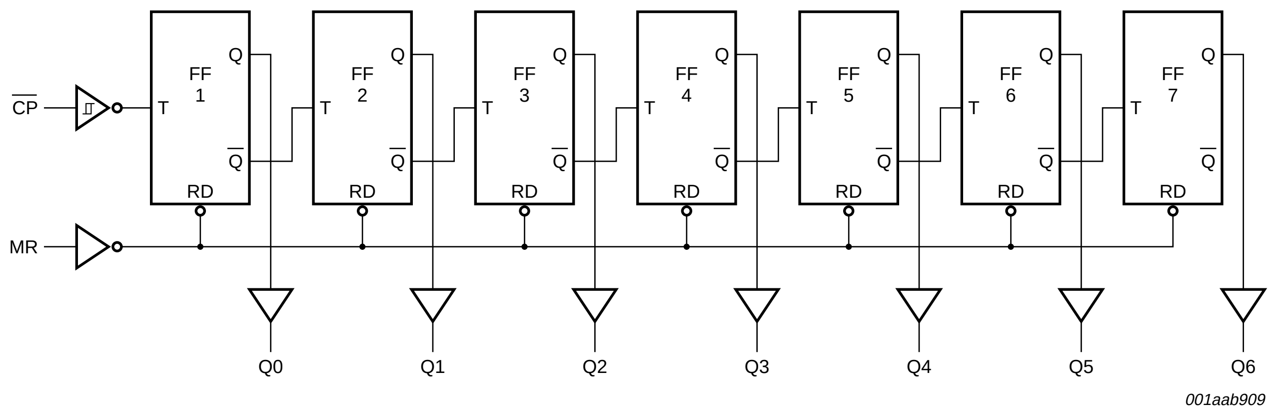


Fig 4. Logic diagram

7. Pinning information

7.1 Pinning

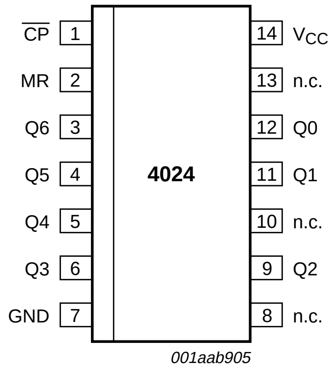


Fig 5. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{CP}$	1	clock input (HIGH-to-LOW, edge-triggered)
MR	2	master reset input (active HIGH)
Q6	3	parallel output 6
Q5	4	parallel output 5
Q4	5	parallel output 4
Q3	6	parallel output 3
GND	7	ground (0 V)
n.c.	8	not connected
Q2	9	parallel output 2
n.c.	10	not connected
Q1	11	parallel output 1
Q0	12	parallel output 0
n.c.	13	not connected
V_{CC}	14	positive supply voltage

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input		Output
MR	**$\overline{CP}$**	**Qn**
H	X	L
L	↑	no change
	↓	count

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW clock transition.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output source or sink current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	DIP14 package	[1]	-	750	mW
	SO14, SSOP14 and TSSOP14 packages	[2]	-	500	mW

[1] Above 70 °C: P_{tot} derates linearly with 12 mW/K.

[2] Above 70 °C: P_{tot} derates linearly with 8 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall times except $\overline{CP}$	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
T_{amb}	ambient temperature		–40	-	+125	°C

11. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	μA

12. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 6				
		$V_{CC} = 2.0$ V	-	47	175	ns
		$V_{CC} = 4.5$ V	-	17	35	ns
		$V_{CC} = 6.0$ V	-	14	30	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	14	-	ns
	propagation delay Qn to Qn+1	see Figure 6				
		$V_{CC} = 2.0$ V	-	25	80	ns
		$V_{CC} = 4.5$ V	-	9	16	ns
		$V_{CC} = 6.0$ V	-	7	14	ns
t_{PHL}	propagation delay MR to Q0	see Figure 6				
		$V_{CC} = 2.0$ V	-	63	200	ns
		$V_{CC} = 4.5$ V	-	23	40	ns
		$V_{CC} = 6.0$ V	-	18	34	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
t_W	$\overline{CP}$ clock pulse width HIGH or LOW	see Figure 6				
		$V_{CC} = 2.0$ V	80	17	-	ns
		$V_{CC} = 4.5$ V	16	6	-	ns
		$V_{CC} = 6.0$ V	14	5	-	ns
	MR master reset pulse width HIGH	see Figure 6				
		$V_{CC} = 2.0$ V	80	22	-	ns
		$V_{CC} = 4.5$ V	16	8	-	ns
		$V_{CC} = 6.0$ V	14	6	-	ns
t_{rem}	removal time MR to $\overline{CP}$	see Figure 6				
		$V_{CC} = 2.0$ V	50	6	-	ns
		$V_{CC} = 4.5$ V	10	2	-	ns
		$V_{CC} = 6.0$ V	9	2	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		$V_{CC} = 2.0$ V	6.0	27	-	MHz
		$V_{CC} = 4.5$ V	30	82	-	MHz
		$V_{CC} = 6.0$ V	35	98	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	90	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [1]	-	25	-	pF

Table 8: Dynamic characteristics *...continued*
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	220	ns
		$V_{CC} = 4.5$ V	-	-	44	ns
		$V_{CC} = 6.0$ V	-	-	37	ns
	propagation delay Qn to Qn+1	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	100	ns
		$V_{CC} = 4.5$ V	-	-	20	ns
		$V_{CC} = 6.0$ V	-	-	17	ns
t_{PHL}	propagation delay MR to Q0	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	250	ns
		$V_{CC} = 4.5$ V	-	-	50	ns
		$V_{CC} = 6.0$ V	-	-	43	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	95	ns
		$V_{CC} = 4.5$ V	-	-	19	ns
		$V_{CC} = 6.0$ V	-	-	16	ns
t_W	$\overline{CP}$ clock pulse width HIGH or LOW	see Figure 6				
		$V_{CC} = 2.0$ V	100	-	-	ns
		$V_{CC} = 4.5$ V	20	-	-	ns
		$V_{CC} = 6.0$ V	17	-	-	ns
	MR master reset pulse width HIGH	see Figure 6				
		$V_{CC} = 2.0$ V	100	-	-	ns
		$V_{CC} = 4.5$ V	20	-	-	ns
		$V_{CC} = 6.0$ V	17	-	-	ns
t_{rem}	removal time MR to $\overline{CP}$	see Figure 6				
		$V_{CC} = 2.0$ V	65	-	-	ns
		$V_{CC} = 4.5$ V	13	-	-	ns
		$V_{CC} = 6.0$ V	11	-	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		$V_{CC} = 2.0$ V	4.8	-	-	MHz
		$V_{CC} = 4.5$ V	24	-	-	MHz
		$V_{CC} = 6.0$ V	28	-	-	MHz

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 6				
		V_{CC} = 2.0 V	-	-	265	ns
		V_{CC} = 4.5 V	-	-	53	ns
		V_{CC} = 6.0 V	-	-	45	ns
	propagation delay Qn to Qn+1	see Figure 6				
		V_{CC} = 2.0 V	-	-	120	ns
		V_{CC} = 4.5 V	-	-	24	ns
		V_{CC} = 6.0 V	-	-	20	ns
t_{PHL}	propagation delay MR to Q0	see Figure 6				
		V_{CC} = 2.0 V	-	-	300	ns
		V_{CC} = 4.5 V	-	-	60	ns
		V_{CC} = 6.0 V	-	-	51	ns
t_{THL}, t_{TLH}	output transition time	see Figure 6				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	$\overline{CP}$ clock pulse width HIGH or LOW	see Figure 6				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
	MR master reset pulse width HIGH	see Figure 6				
		V_{CC} = 2.0 V	120	-	-	ns
		V_{CC} = 4.5 V	24	-	-	ns
		V_{CC} = 6.0 V	20	-	-	ns
t_{rem}	removal time MR to $\overline{CP}$	see Figure 6				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns
f_{max}	maximum clock frequency	see Figure 6				
		V_{CC} = 2.0 V	4.0	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

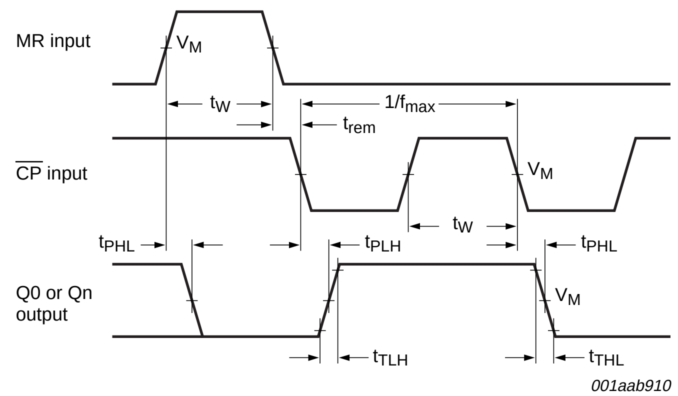
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

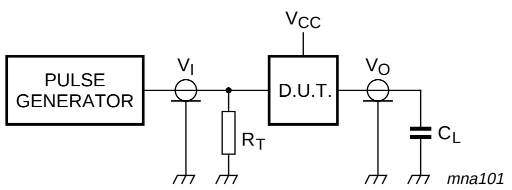
13. Waveforms



Also showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

$V_M = 0.5 \times V_I$.

Fig 6. Waveforms showing the clock ($\overline{CP}$) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

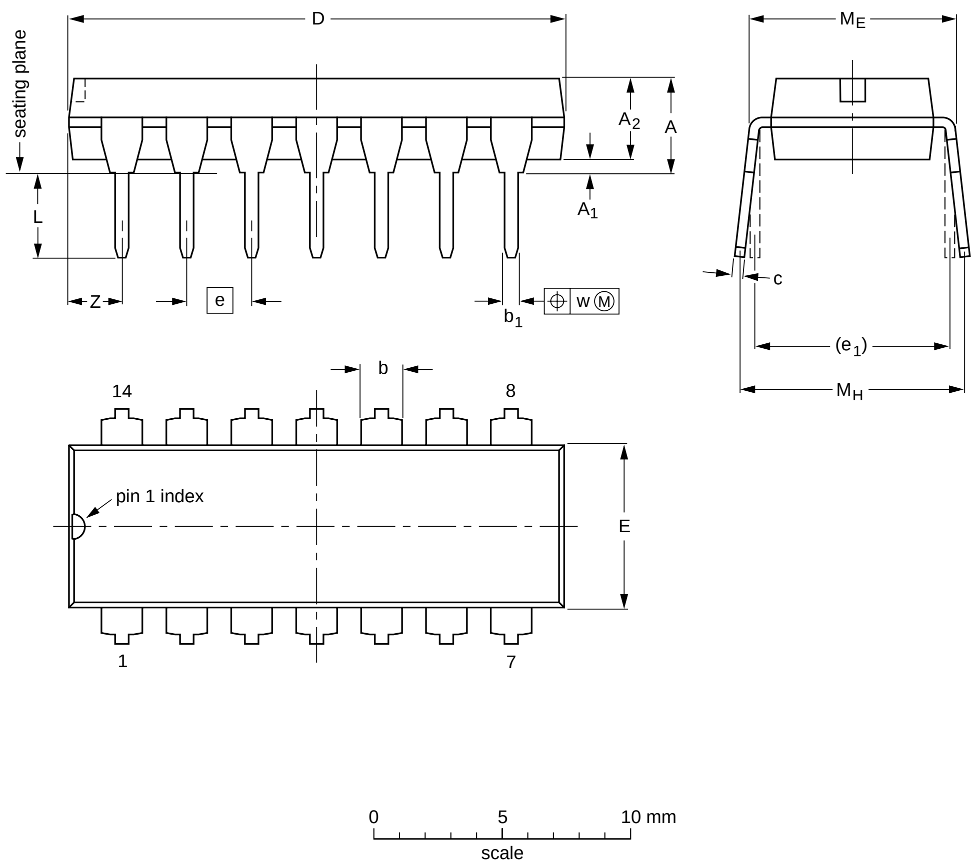
Fig 7. Load circuitry for switching times

Table 9: Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

14. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

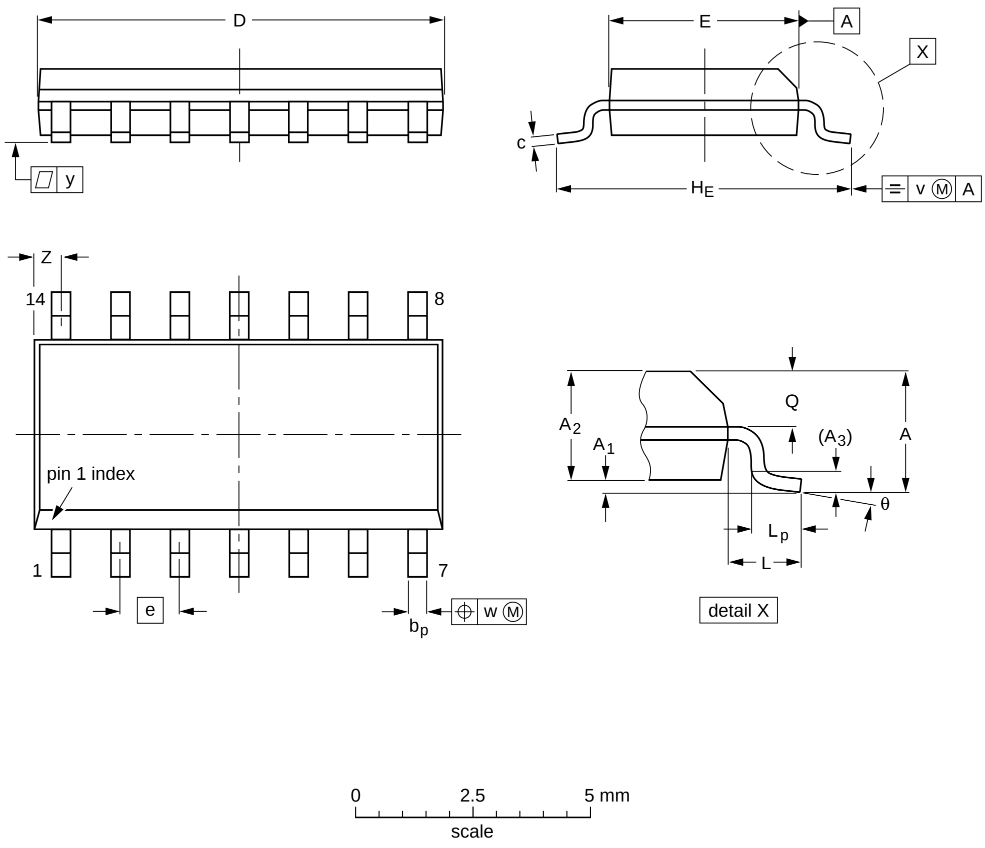
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

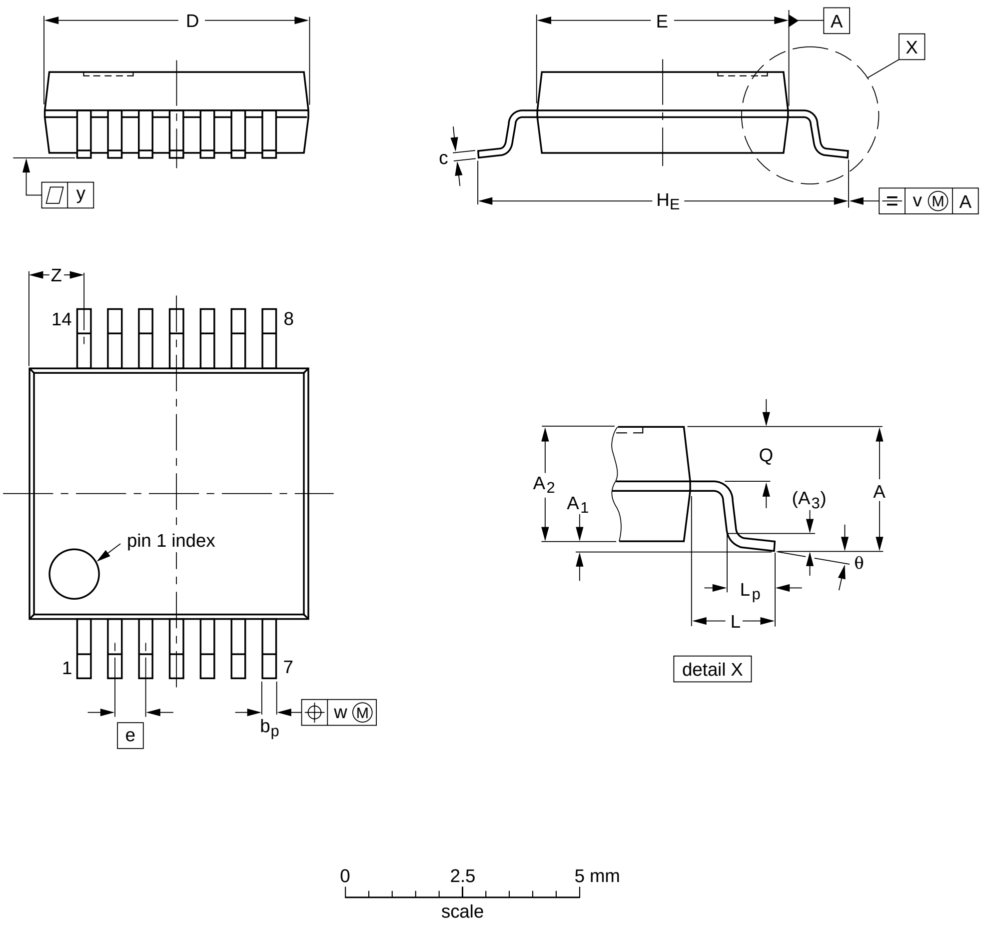
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

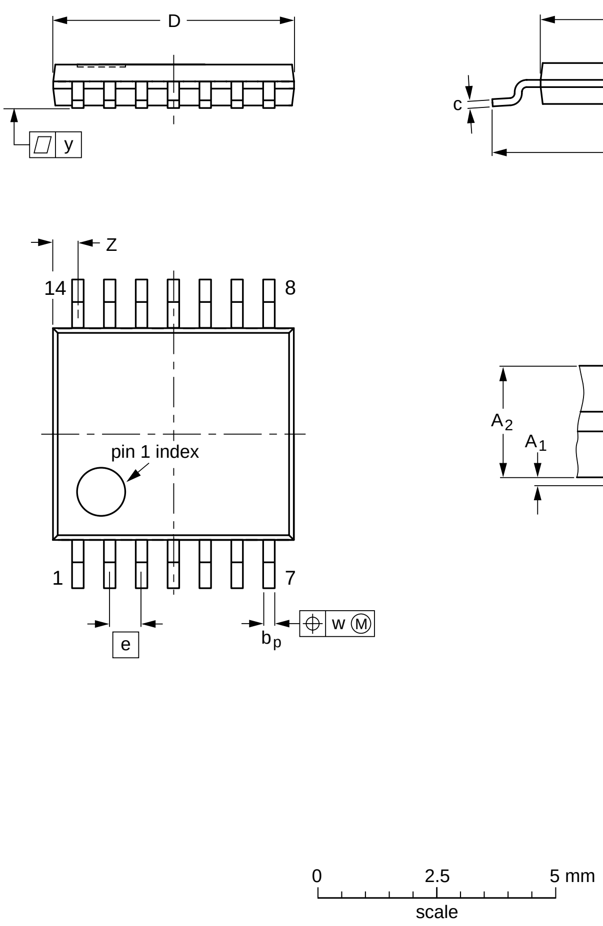
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(2)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

15. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC4024_3	20041112	Product data sheet	-	9397 750 13813	74HC_HCT4024_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT4024. • Inserted family specification.				
74HC_HCT4024_CNV_2	19970901	Product specification	-	-	74HC_HCT4024_1
74HC_HCT4024_1	19901201	Product specification	-	-	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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